REGULATOR CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2016-015849; filed on January 29, 2016; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a regulator circuit.

BACKGROUND

Recently, a portable electronic apparatus has been developed, and thus, it is necessary to further reduce current consumption of a low dropout (LDO) linear regulator circuit. However, if the current consumption of the linear regulator circuit is reduced, it is not possible to supply a sufficient current to a load, when an operation state of the load is rapidly changed. Accordingly, if the current consumption is excessively reduced, the linear regulator circuit does not cope with a rapid change of an output voltage in a short time.

An example of related art includes JP-A-2012-15927 (U.S. Patent No. 8665020).

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram illustrating an example of a configuration of a regulator circuit according to a first embodiment.

FIG. 2 is a diagram illustrating an example of a configuration of a regulator circuit according to a second embodiment.

FIG. 3 is a diagram illustrating an example of a configuration of the regulator circuit according to a modification example 1 of the first embodiment.

FIG. 4 is a diagram illustrating an example of a configuration of the regulator circuit according to a modification example 2 of the second embodiment.

DETAILED DESCRIPTION

[0004]One embodiment is to provide a regulator circuit which consumes a small current and can cope with a rapid change of an output voltage in a short time.

[0005]In general, according to one embodiment, a regulator circuit includes a comparison unit which outputs a differential voltage based on a difference between a first voltage that is obtained by dividing an output voltage, and a reference voltage. An amplification unit amplifies the differential voltage. A supply unit supplies a current according to an output of the amplification unit to a load. A current source is connected between the amplification unit and the supply unit, and increases a current flowing through the amplification unit, based on the output voltage.

[0007]Hereinafter, exemplary embodiments will be described with reference to the accompanying drawings. The invention is not limited to the present embodiment.

First Embodiment

[0008]FIG. 1 is a diagram illustrating an example of a configuration of a linear regulator circuit 1 (hereinafter, referred to as a regulator circuit 1) according to a first embodiment. The regulator circuit 1 includes an output node Nout which can be connected to a load 2, and applies an output voltage Vout to the load 2 from the output node Nout. The output node Nout may be, for example, a pad or a terminal. The load 2 is, for example, a portable electronic apparatus or a part thereof, and consumes small power at the time of a stop state (OFF state of stand-by state), but consumes relatively large power at the time of a start-up state. When the load 2 is changed from a stop state into a start-up state, large power is rapidly required. For example, since it is preferable that a camera function or the like of a smart phone starts up in a short time if possible, it is necessary for the regulator circuit 1 to increase a supply current from the output node Nout in a short time at the time of start-up of the camera function. The instantaneous increase of a supply current causes an excessive decrease of an output voltage Vout. Hence, in order for the regulator circuit 1 to prevent an excessive decrease of the output voltage Vout at the time of start-up of the load 2, it is preferable to quickly follow up a change of the output voltage Vout. Meanwhile, in order for an output capacitor Co to supply a current to the load 2 at the time of an excessive decrease of the output voltage Vout, the output capacitor Co is connected between the output node Nout and a ground GND. However, only the output capacitor Co cannot sufficiently prevent the output voltage Vout from decreasing when large power is rapidly required. Accordingly, the regulator circuit 1 connected to the load 2 has the following configuration.

[0009]The regulator circuit 1 includes a comparison unit CMP, an amplification unit AMP, a supply unit SUP, an auxiliary current source SRC, and voltage dividing resistance elements R3 and R4.

[0010]The comparison unit CMP may be, for example, a differential amplification circuit (operational amplifier). A non-inverting input of the comparison unit CMP is connected to a power supply 4 which generates a reference voltage Vref. The power supply 4 supplies the reference voltage Vref to the regulator circuit 1 through a power supply pad (not illustrated). Alternatively, the power supply 4 may be embedded in a chip of the regulator circuit 1. An inverting input of the comparison unit CMP is connected between the voltage dividing resistance elements R3 and R4. The voltage dividing resistance elements R3 and R4 are connected in series between the output node Nout and a second power supply line Lgnd, divide the output voltage Vout, and generate a monitor voltage (first voltage, feedback voltage) Vmon which is approximately proportional to the output voltage Vout. The comparison unit CMP receives the monitor voltage Vmon and the reference voltage Vref, and outputs a differential voltage Vdff based on a difference between the monitor voltage Vmon and the reference voltage Vref. The comparison unit CMP may output a voltage difference between the monitor voltage Vmon and the reference voltage Vref as the differential voltage Vdff, or may output the voltage difference which is amplified as the differential voltage Vdff.

[0011]The amplification unit AMP includes a first transistor M1 and a second transistor M2 which are connected in series between a first power supply line Lvdd and a second power supply line Vgnd. The first power supply line Lvdd is a wire which can be connected to a voltage source which supplies, for example, a high level voltage VDD. The second power supply line Lgnd is a wire which can be connected to a voltage source which supplies, for example, a low level voltage GND (for example, a ground voltage).

[0012]The first transistor M1 is, for example, a p-type metal insulator semiconductor field effect transistor (MISFET). A gate of the first transistor M1 is connected to an output of the comparison unit CMP, and receives the differential voltage Vdff. A drain of the first transistor M1 is connected to the first power supply line Lvdd, and a source of the first transistor M1 is connected to a first node N1.

[0013]The second transistor M2 is, for example, an n-type MISFET. A gate of the second transistor M2 receives a constant voltage Vcnst. A drain of the second transistor M2 is connected to the first node N1, and is connected to the source of the first transistor M1 through the first node N1. A source of the second transistor M2 is connected to the second power supply line Lgnd.

[0014]The first transistor M1 controls electrical resistance between the first node N1 and the first power supply line Lvdd, based on the differential voltage Vdff, and changes a current. The second transistor M2 receives the constant voltage Vcnst and supplies a constant current to the first transistor M1. That is, the second transistor M2 functions as a constant current source. For example, in a case where the monitor voltage Vmon is lower than the reference voltage Vref, the differential voltage Vdff becomes a positive voltage, and thereby the first transistor M1 is turned off. Hence, a current flowing from the first power supply line Lvdd to the first node N1 decreases, and a constant current flows through the second transistor M2 from the first node N1. By doing so, a voltage of the first node N1 decreases. At this time, the auxiliary current source SRC also supplies a current, but a function of the auxiliary current source SRC will be described below. Meanwhile, in a case where the monitor voltage Vmon is higher than the reference voltage Vref, the differential voltage Vdff becomes a negative voltage, and thereby the first transistor M1 is turned on. Hence, a current flowing from the first power supply line Lvdd to the first node N1 increases. At this time, a constant current continuously flows through the second transistor M2, but a current from the first power supply line Lvdd is much larger than a constant current flowing through the second transistor M2, and thereby a voltage of the first node N1 increases. Accordingly, the differential voltage Vdff is amplified between the high level voltage VDD and the low level voltage GND, in the first node N1, and is output to the supply unit SUP.

[0015]The supply unit SUP includes a third transistor M3. The third transistor M3 is, for example, a p-type MISFET. A gate of the third transistor M3 is connected to the first node N1, and receives a voltage which is amplified by the amplification unit AMP. A source of the third transistor M3 is connected to the first power supply line Lvdd. A drain of the third transistor M3 is connected to the output node Nout, and is connected to the second power supply line Lgnd through the voltage dividing resistance elements R3 and R4. That is, a voltage from the third transistor M3 is applied to the load 2 as the output voltage Vout.

[0016]The third transistor M3 controls electrical resistance between the output node Nout and the first power supply line Lvdd, based on a voltage of the first node N1, and changes a current. Accordingly, the third transistor M3 supplies a current according to an output (that is, a voltage of the first node N1) of the amplification unit AMP to the load 2. For example, in a case where the monitor voltage Vmon is lower than the reference voltage Vref and a voltage of the first node N1 approaches the low level voltage GND, the third transistor M3 is turned on. Hence, a current flowing from the first power supply line Lvdd to the output node Nout increases. Accordingly, power is supplied to the load 2. Meanwhile, in a case where the monitor voltage Vmon is higher than the reference voltage Vref and the voltage of the first node N1 approaches the high level voltage VDD, the third transistor M3 is turned off. Hence, a current flowing from the first power supply line Lvdd to the output node Nout decreases, and a voltage of the output node Nout approaches a voltage of the second power supply line Lgnd through the voltage dividing resistance elements R3 and R4. Accordingly, power which is supplied to the load 2 decreases. In this way, the regulator circuit 1 feeds back the output voltage Vout as the monitor voltage Vmon, supplies a current to the output node Nout in a case where the output voltage Vout is relatively low, and stops supplying the current to the output node Nout in a case where the output voltage Vout is relatively high. Accordingly, the regulator circuit 1 operates so as to maintain the output voltage Vout as an approximately constant voltage.

[0017]The auxiliary current source SRC includes a fourth transistor M4, a first resistance element R1, a first capacitor C1, and a second resistance element R2. The fourth transistor M4 is, for example, an n-type MISFET. A gate of the fourth transistor M4 receives the constant voltage Vcnst in common with the gate of the second transistor M2. A drain of the fourth transistor M4 is connected to the first node N1, and a source of the fourth transistor M4 is connected to a second node N2. The first resistance element R1 is connected between the second node N2 and the second power supply line Lgnd. That is, the fourth transistor M4 and the first resistance element R1 are connected in series between the first node N1 and the second power supply line Lgnd. The first capacitor C1 is electrically connected between the second node N2 and the output node Nout, and the second resistance element R2 is electrically connected between the first capacitor C1 and the output node Nout. That is, the first capacitor C1 and the second resistance element R2 are connected in series between the second node N2 and the output node Nout. The second resistance element R2 is effective in a case where a breakable element such as a MOS capacitor is used as the first capacitor C1. Meanwhile, a “connection” includes not only a direct connection but also an electrical connection, and other elements, wires, or the like may be interposed between the elements which are connected to each other.

[0018]A gate of the fourth transistor M4 receives the constant voltage Vcnst in the same manner as the gate of the second transistor M2. However, A source of the fourth transistor M4 is connected to the second power supply line Lgnd through the first resistance element R1, and thereby a source voltage becomes a higher voltage than the low level voltage GND by the first resistance element R1, if the output voltage Vout does not drop a voltage of the second node N2. That is, a source voltage of the fourth transistor M4 can be set to a higher voltage than a source voltage of the second transistor M2. Accordingly, the fourth transistor M4 receives the constant voltage Vcnst in common with the second transistor M2 and performs control, but the second transistor M2 is approximately turned on, and the fourth transistor M4 can be maintained in a turn-off state. For example, in a case where the load 2 is in a state (normal operation state) of normally starting up, the regulator circuit 1 stabilizes the output voltage Vout to a certain voltage, such that the monitor voltage Vmon is fed back and the monitor voltage Vmon approaches the reference voltage Vref. In this case, in a case where the monitor voltage Vmon is equal to the reference voltage Vref, if the differential voltage Vdff outputs a normal value, a voltage difference between the differential voltage Vdff and the normal value becomes approximately zero or a small value as an absolute value. A voltage of the first node N1 is determined by the differential voltage Vdff and a constant current flowing through the second transistor M2, and turn-on or turn-off of the third transistor M3 is determined by a voltage of the first node N1. The output voltage Vout is maintained in the certain voltage by turn-on of the third transistor M3. Meanwhile, when the load 2 is in a normal operation state, a source voltage of the fourth transistor M4 is higher than that of the second transistor M2, and thereby the fourth transistor M4 is maintained in an approximately turn-off state. Accordingly, in a case where the load 2 is in the normal operation state, a current from the first node N1 flows through the second transistor M2, but the current from the first node N1 does not mostly flow through the fourth transistor M4.

[0019]Meanwhile, in a case where the load 2 is changed from a stop state into a start-up state, the output voltage Vout can decrease rapidly and significantly as described above. In this case, the excessively decreased output voltage Vout is transferred to the second node N2 though the second resistance element R2 and the first capacitor C1, and significantly decreases the source voltage of the fourth transistor M4. Accordingly, shortly after the output voltage Vout rapidly decreases, the fourth transistor M4 is approximately turned on in a shorter time than time taken to feedback-control the monitor voltage Vmon. A current flows through the second transistor M2 and the fourth transistor M4 from the first node N1, and thus, a current flowing through the amplification unit AMP is amplified, and a voltage (gate voltage of the third transistor M3) of the first node N1 can decrease in a short time.

[0020]In this way, the auxiliary current source SRC is connected between the amplification unit AMP the supply unit SUP, and a current flowing through the amplification unit AMP increases based on the output voltage Vout, as will be described below. Meanwhile, the second resistance element R2 may not be provided.

[0021]Subsequently, an operation of the regulator circuit 1 will be described.

Case Where Load 2 is in Normal Operation State

[0022]In a case where the load 2 is maintained in a start-up state and is in a normal operation state, the output voltage Vout is relatively stable, and the monitor voltage Vmon is stable in the vicinity of the reference voltage Vref. At this time, as described above, the fourth transistor M4 is nearly in a turn-off state, and the auxiliary current source SRC does not nearly amplify a current of the amplification unit AMP. Meanwhile, the differential voltage Vdff which is output from the comparison unit CMP has a relatively small value as an absolute value, compared to a certain normal value. Accordingly, the first transistor M1 repeats an approximately turn-on state and an approximately turn-off state, such that the monitor voltage Vmon is approximately equal to the reference voltage Vref, or enters a turn-on state (half turn-on state) between the turn-on state and the turn-off state. The current from the first node N1 flows through the second transistor M2, and thus, the voltage of the first node N1 depends upon the turn-on (approximately turn-on state to approximately turn-off state) of the first transistor M1. The third transistor M3 enters a turn-off state (approximately turn-on state to approximately turn-off state) according to the voltage of the first node N1, and adjusts the output voltage Vout. In this way, when the load 2 is in the normal operation state, the regulator circuit 1 feeds back the monitor voltage Vmon of the output voltage Vout to the comparison unit CMP, and controls the output voltage Vout such that the monitor voltage Vmon is equal to the reference voltage Vref. In this case, the output voltage Vout does not change rapidly or significantly, and thus, a current does not nearly flow through the auxiliary current source SRC.

Case Where Load 2 is Changed from Stop State to Start-up State

[0023]In a case where the load 2 is in the stop state, current consumption of the load 2 is significantly reduced. Even in this case, the regulator circuit 1 adjusts the output voltage Vout such that the monitor voltage Vmon is equal to the reference voltage Vref. At this time, a current does not mostly flow through the auxiliary current source SRC in the same manner as in the normal operation state.

[0024]In a case where the load 2 is changed from the stop state to the start-up state, current consumption of the load 2 is rapidly increased. In this case, the output voltage Vout decreases excessively and significantly. The decreased output voltage Vout is transferred to the second node N2 through the second resistance element R2 and the first capacitor C1, and a source voltage of the fourth transistor M4 significantly decreases. Accordingly, as described above, shortly after the output voltage Vout rapidly decreases, the fourth transistor M4 enters an approximately turn-on state. The source of the fourth transistor M4 nearly directly receive the output voltage Vout from the output node Nout through the second resistance element R2 and the first capacitor C1, and thus, the fourth transistor M4 operates more quickly than that at the time of feedback control (comparison unit CMP and first transistor M1) of the regulator circuit 1. Hence, the fourth transistor M4 quickly decreases the voltage of the first node N1, and operates the third transistor M3 in a short time from an excessive decrease of the output voltage Vout. Accordingly, the third transistor M3 can quickly recover the output voltage Vout.

[0025]Thereafter, the load 2 maintains the start-up state, and if the output voltage Vout is relatively stabilized, the monitor voltage Vmon is stabilized in the vicinity of the reference voltage Vref. Accordingly, the load 2 enters the normal operation state.

[0026]In this way, according to the present embodiment, the auxiliary current source SRC increases the current flowing through the amplification unit AMP, based on the output voltage Vout, when the load 2 is changed from the stop state. Accordingly, the regulator circuit 1 can quickly recover the output voltage Vout to cope with an excessive decrease of vout in a short time, even though current drive capability of the second transistor M2 is small.

[0027]Meanwhile, a current from amp does not mostly flow through the auxiliary current source SRC, when the load 2 is in the normal operation state. Hence, after the load 2 is changed from the stop state to the start-up state, if the load 2 enters the normal operation state and the output voltage Vout is stabilized, a current flows through the second transistor M2 of the amplification unit AMP, but the current does not nearly flow through the fourth transistor M4, in the regulator circuit 1. Accordingly, it is possible to sufficiently reduce the current drive capability of the second transistor M2, and to maintain the entire current consumption of the regulator circuit 1 in a small amount (for example, equal to or less than 1 mA).

[0028]Furthermore, the regulator circuit 1 According to the present embodiment includes a feedback circuit (the comparison unit CMP, the amplification unit AMP, and the supply unit SUP) which controls the output voltage Vout by feeding back the monitor voltage Vmon according to the output voltage Vout, such that the monitor voltage Vmon is equal to the reference voltage Vref. Accordingly, when the load 2 is in the normal operation state, the regulator circuit 1 can be stabilized by control the output voltage Vout such that the monitor voltage Vmon is equal to the reference voltage Vref.

[0029]In a case where the auxiliary current source SRC is not provided, the feedback function is effectively performed by using the comparison unit CMP and the first transistor M1, but when a current which is consumed by the load 2 rapidly changes, transient response characteristics of the output voltage Vout are degraded. In this case, if a current flowing through a regulator circuit increases, it is possible to improve the transient response characteristics of the output voltage Vout. However, it is not preferable to increase a current which is consumed in the regulator circuit which requires low power consumption, such as a portable electronic apparatus. Hence, it is difficult to satisfy both low current consumption and improved transient response characteristics of the regulator circuit which is employed in the portable electronic apparatus or the like.

[0030]In contrast to this, the regulator circuit 1 according to the present embodiment provides the auxiliary current source SRC, and thereby a current flowing through the amplification unit AMP does not increase when the load 2 is in the normal operation state, and the current flowing through the amplification unit AMP increases when the load 2 is changed from a stop state to a start-up state. Accordingly, the regulator circuit 1 can reduce power consumption and improve the transient response characteristics of the output voltage Vout.

Second Embodiment

[0031]FIG. 2 is a diagram illustrating an example of a configuration of a regulator circuit 10 according to a second embodiment. The second embodiment is different from the first embodiment in that the second embodiment includes a fifth transistor M5 which functions as the first resistance element. Other configurations of the second embodiment may be the same as the configurations of the first embodiment corresponding thereto.

[0032]The fifth transistor M5 is, for example, an n-type MISFET. A gate of the fifth transistor M5 receives a constant voltage in common with the gate of the fourth transistor M4. A drain of the fifth transistor M5 is connected to the second node N2, and a source of the fifth transistor M5 is connected to the second power supply line Lgnd.

[0033]When the load 2 is in the normal operation state, the fifth transistor M5 may be in an approximately turn-on state. In this case, if the fifth transistor M5 is designed such that ON resistance of the fifth transistor M5 is equal to resistance of the second resistance element R2 according to the first embodiment, the fourth transistor M4 is approximately turned off when the load 2 is in the normal operation state. Meanwhile, the source of the fourth transistor M4 is connected to the output node Nout through the first capacitor C1 and the second resistance element R2. Hence, the fourth transistor M4 increases a current flowing through the amplification unit AMP when the load 2 is changed from the stop state to start-up state. Hence, the regulator circuit 10 can perform the same operation as the regulator circuit 1 according to the first embodiment. Accordingly, the second embodiment can obtain the same effects as the first embodiment.

Modification Example 1

[0034]FIG. 3 is a diagram illustrating an example of a configuration of the regulator circuit 1 according to a modification example 1 of the first embodiment. In the present modification example, the first capacitor C1 is not connected between the output node Nout and the second node N2, but connected between a third node N3 and the second node N2. The third node N3 is a node connected between the voltage dividing resistance element R3 and the voltage dividing resistance element R4. Meanwhile, in the present modification example, the voltage dividing resistance element R3 may be said to have both a voltage division function of the output voltage Vout and a function of the second resistance element R2.

[0035]Accordingly, the auxiliary current source SRC increases a current flowing through the amplification unit AMP by using the monitor voltage Vmon according to the output voltage Vout. The monitor voltage Vmon is obtained by dividing the output voltage Vout using the voltage dividing resistance elements R3 and R4, and thus, the monitor voltage Vmon corresponds to the output voltage Vout. Hence, the regulator circuit 1 according to the present modification example can also increase the current flowing through the amplification unit AMP, based on the output voltage Vout, in a case where the load 2 is changed from the stop state to the start-up state. That is, the present modification example can operate in the same manner as the first embodiment.

Modification Example 2

[0036]FIG. 4 is a diagram illustrating an example of a configuration of the regulator circuit 10 according to a modification example 2 of the second embodiment. The modification example 2 is a modification example in which the modification example 1 is applied to the second embodiment. Also in the modification example 2, the first capacitor C1 is connected between the third node N3 and the second node N2. Accordingly, the auxiliary current source SRC increases the current flowing through the amplification unit AMP by using the monitor voltage Vmon according to the output voltage Vout. Hence, the regulator circuit 10 according to the modification example 2 can also increase the current flowing through the amplification unit AMP, based on the output voltage Vout, in a case where the load 2 is changed from the stop state to the start-up state. That is, the modification example 2 can operate in the same manner as the second embodiment.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A regulator circuit comprising:

a comparison unit which outputs a differential voltage based on a difference between a first voltage that is obtained by dividing an output voltage, and a reference voltage;

an amplification unit which amplifies the differential voltage;

a supply unit which supplies a current according to an output of the amplification unit to a load; and

a current source which is connected between the amplification unit and the supply unit, and increases a current flowing through the amplification unit, based on the output voltage.

2. The circuit according to Claim 1,

wherein the amplification unit includes first and second transistors which are connected in series between a first power supply line and a second power supply line,

wherein a gate of the first transistor is connected to an output of the comparison unit,

wherein a gate of the second transistor receives a constant voltage,

wherein the supply unit includes a third transistor which is connected between the first power supply line and the second power supply line, and

wherein a gate of the third transistor is connected to a first node between the first transistor and the second transistor.

3. The circuit according to Claim 2, wherein the current source includes

a fourth transistor and a first resistance element which are connected in series between the first node and the second power supply line; and

a first capacitor which is connected between a second node between the fourth transistor and the first resistance element, and an output of the supply unit.

4. The circuit according to Claim 3, wherein a gate of the fourth transistor receives the constant voltage in common with the gate of the third transistor.

5. The circuit according to Claim 3 or 4, wherein the current source further includes a second resistance element which is provided between the first capacitor and the output of the supply unit.

6. The circuit according to any one of Claims 3 to 5, wherein the first resistance element is a fifth transistor whose gate receives the constant voltage in common with the gate of the fourth transistor.

7. A regulator circuit comprising:

a comparison unit which receives a first voltage that is obtained by dividing a voltage of an output node, and a reference voltage;

a first transistor which has a gate that is connected to an output of the comparison unit, a drain that is connected to a first power supply line, and a source that is connected to a first node;

a second transistor which has a gate that receives a constant voltage, a drain that is connected to the first node, and a source that is connected to a second power supply line;

a third transistor which has a gate that is connected to the first node, a source that is connected to the first power supply line, and a drain that is connected to the output node;

a fourth transistor which has a gate that receives the constant voltage, a drain that is connected to the first node, and a source that is connected to a second node;

a first resistance element which is connected between the second node and the second voltage source; and

a first capacitor which is connected between the second node and the output node.

ABSTRACT

According to one embodiment, a regulator circuit includes a comparison unit which outputs a differential voltage based on a difference between a first voltage that is obtained by dividing an output voltage, and a reference voltage. An amplification unit amplifies the differential voltage. A supply unit supplies a current according to an output of the amplification unit to a load. A current source is connected between the amplification unit and the supply unit, and increases a current flowing through the amplification unit, based on the output voltage.